

CLAIMS

We claim:

- 1 1. A process of forming a nitride film on a
2 semiconductor substrate, comprising:
3 exposing a surface of the substrate to a rapid thermal
4 process to form the nitride film.

- 1 2. The process according to claim 1, wherein the
2 nitride film is a silicon nitride film for selectively
3 blocking silicide formation for a resistor, and wherein the
4 rapid thermal process comprises exposing a surface of a doped
5 polycrystalline silicon region or doped silicon region to a
6 rapid thermal nitride deposition.

- 1 3. The process according to claim 2, wherein the
2 silicon nitride film has a thickness of about 100 Å or less.

- 1 4. The process according to claim 2, wherein the rapid
2 thermal nitride deposition comprises:
3 exposing the doped polycrystalline silicon region or
4 doped silicon region to a temperature above about 700°C for a
5 period of time of about two minutes or less.

1 5. The process according to claim 4, wherein the
2 silicon nitride film has a thickness of about 100 Å or less.

1 6. The process according to claim 2, wherein the rapid
2 thermal nitride deposition is carried out in a processing
3 chamber at a temperature of about 775°C, at a pressure of
4 about 100 torr, with the semiconductor substrate is rotated
5 at a rate of about 35 rpm, and with SiH₄ and NH₃ gasses being
6 introduced into the processing chamber at a ratio of about
7 40:4.

1 7. The process according to claim 1, wherein the rapid
2 thermal process comprises a rapid thermal chemical vapor
3 deposition.

1 8. The process according to claim 7, wherein the rapid
2 thermal chemical vapor deposition is carried out at a
3 temperature of about 700°C to about 750°C for a period of
4 time of about 30 seconds to about 5 minutes.

1 9. The process according to claim 7, wherein the
2 barrier nitride film has a thickness of about 100 Å to about
3 150 Å.

1 10. The process according to claim 7, wherein the
2 nitride film comprises a barrier to oxidation for a bipolar
3 transistor.

1 11. The process according to claim 7, wherein the
2 nitride film comprises a conformal film.

1 12. The process according to claim 11, wherein the
2 nitride film comprises a barrier on a CMOS FET.

1 13. The process according to claim 11, wherein the
2 rapid thermal chemical vapor deposition is carried out at a
3 temperature of about 600°C to about 800°C.

1 13. The process according to claim 11, wherein the
2 rapid thermal chemical vapor deposition is carried out at a
3 temperature of about 600°C to about 700°C.

1 14. The process according to claim 11, wherein the
2 rapid thermal chemical vapor deposition is carried out at a
3 temperature of about 700°C to about 710°C.

1 15. The process according to claim 11, wherein the

2 rapid thermal chemical vapor deposition is carried out at a
3 temperature of about 700°C.

1 16. The process according to claim 11, wherein the
2 rapid thermal chemical vapor deposition is carried out at a
3 temperature of about 700°C to about 775°C.

1 17. The process according to claim 11, wherein the
2 rapid thermal chemical vapor deposition is carried out at a
3 temperature of about 680°C or greater.

1 18. The process according to claim 17, wherein the
2 process is carried out at a pressure of about 100 torr.

1 19. The process according to claim 11, wherein the
2 rapid thermal chemical vapor deposition is carried out for a
3 period of time of about 1 minute to about 4 minutes.

1 20. The process according to claim 11, wherein the
2 film has a conformality of greater than about 90%.

1 21. The process according to claim 11, wherein the
2 film has a conformality of about 95% to about 100%.

1 22. The process according to claim 11, wherein the
2 process is carried out at a pressure of about 100 torr.

1 23. The process according to claim 11, wherein the
2 process is carried out at a pressure of about 250 torr or
3 greater.

1 24. The process according to claim 11, wherein the
2 process is carried out at a pressure of about 100 torr to
3 about 250 torr.

1 25. The process according to claim 11, further
2 comprising introducing NH_3 gas into a processing chamber that
3 the rapid thermal chemical vapor deposition is carried out
4 in.

1 26. The process according to claim 25, wherein the NH_3
2 gas is introduced into the processing chamber at a rate of
3 about 4 liters per minute.

1 27. The process according to claim 11, further
2 comprising introducing SiH_4 gas into a processing chamber
3 that the rapid thermal chemical vapor deposition is carried

4 out in.

1 28. The process according to claim 27, wherein the SiH₄
2 gas is introduced into the processing chamber at a rate of
3 about 40 sccm.

1 29. A method of forming a resistor, comprising:
2 selectively blocking silicide formation over a doped
3 polycrystalline silicon region or doped silicon region by
4 forming a region of a silicon nitride film utilizing a rapid
5 thermal nitride deposition after formation of device
6 source/drain implants and completion of activation anneals;
7 and
8 forming a contact on either side of the blocked region
9 to form a current path through the blocked region.

1 30. A blocked silicide resistor structure, comprising:
2 a silicide blocking region comprising a silicon nitride
3 film arranged over a region of doped polycrystalline silicon
4 or doped silicon, wherein the silicon nitride film has been
5 formed by a rapid thermal nitride deposition;
6 a region of a silicide adjacent opposite sides of the
7 silicon nitride film; and

8 a contact overlying each of the adjacent silicide
9 regions;
10 wherein the resistor overlies device source/drain
11 implants.

1 31. The resistor structure according to claim 30,
2 wherein the adjacent silicide regions include a metal
3 silicide.

1 32. The resistor structure according to claim 30,
2 wherein the metal silicide is selected from the group
3 consisting of titanium silicide and cobalt silicide.

1 33. The resistor structure according to claim 30,
2 wherein the silicon nitride film has a thickness of about 100
3 Å or less.

1 34. The resistor structure according to claim 30,
2 wherein the resistor structure is formed on cobalt silicide
3 based structures.

1 35. A bipolar transistor structure, comprising:
2 a nitride barrier layer formed by a rapid thermal

3 chemical vapor deposition.

1 36. A CMOS FET structure, comprising:

2 a conformal nitride barrier film formed by a rapid

3 thermal nitride deposition.